**Architecture Plan**

Admission system

**Contents**

[**List of table** 2](#_Toc373159013)

[**1.** **Revision** 3](#_Toc373159014)

[**2.** **Introduction** 4](#_Toc373159015)

[2.1. Purpose 4](#_Toc373159016)

[2.2. Goal 4](#_Toc373159017)

[**3.** **ACDM** 5](#_Toc373159018)

[3.1 ACDM 5](#_Toc373159019)

[3.2 ACDM Description 6](#_Toc373159020)

[3.2.1 Stage 1 6](#_Toc373159021)

[3.2.2 Stage 2 7](#_Toc373159022)

[3.2.3 Stage 3 8](#_Toc373159023)

[3.2.4 Stage 4 9](#_Toc373159024)

[3.1.1 Stage 5 10](#_Toc373159025)

[3.1.2 Stage 6 11](#_Toc373159026)

[3.1.3 Stage 7 13](#_Toc373159027)

[3.1.4 Stage 8 14](#_Toc373159028)

[**4.** **Role and Responsibilities** 15](#_Toc373159029)

[4.1 Responsibility 15](#_Toc373159030)

[4.1.1 Managing Engineer 15](#_Toc373159031)

[4.1.2 Chief Architect 15](#_Toc373159032)

[4.1.3 Requirement Engineer 16](#_Toc373159033)

[4.1.4 Chief Scientist 16](#_Toc373159034)

[4.1.5 Quality Process Engineer 17](#_Toc373159035)

[4.1.6 Support Engineer 17](#_Toc373159036)

[4.1.7 Production Engineer 18](#_Toc373159037)

[4.2 Role 18](#_Toc373159038)

# **List of table**

[Table 1: Revision history 3](#_Toc373158996)

[Table 2: Stage description 6](#_Toc373158997)

[Table 3: Stage 2 description 7](#_Toc373158998)

[Table 4: Stage 3 description 8](#_Toc373158999)

[Table 5: Stage 4 description 9](#_Toc373159000)

[Table 6: Stage 5 description 10](#_Toc373159001)

[Table 7: Stage 6 description 12](#_Toc373159002)

[Table 8: Stage 7 description 14](#_Toc373159003)

[Table 9: Stage 8 description 14](#_Toc373159004)

[Table 10: Managing engineer responsibility 15](#_Toc373159005)

[Table 11: Chief Architect responsibility 15](#_Toc373159006)

[Table 12: Requirement Engineer responsibility 16](#_Toc373159007)

[Table 13: Chief Scientist responsibility 17](#_Toc373159008)

[Table 14: Quality Process Engineer responsibility 17](#_Toc373159009)

[Table 15: Support engineer responsibility 18](#_Toc373159010)

[Table 16: Product Engineer responsibility 18](#_Toc373159011)

[Table 17: Role 18](#_Toc373159012)

# **Revision**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No** | **Version** | **Update date** | **Author** | **Content** |
| 1 | 1.0 | 11/20/2013 | Ta Ngoc Thien Phu | Create document |
| 2 | 1.1 | 11/222/2013 | Ta Ngoc Thien Phu | Update document |

Table 1: Revision history

# **Introduction**

## Purpose

* This purpose of this document is show general view about architecture process and guide members how to design architecture in Admission system project

## Goal

* + All members can overview about architecture process
  + Know task that they have to design in architecture phase

# **ACDM**

# ACDM



*Architecture Process*

## ACDM Description

### Stage 1

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
| Establish meetings with the system Stakeholders |  | Establish the encounters between stakeholders and the architectural design team are structured to make the most efficient use of valuable time spent with the stakeholders. |
| Discover Architectural Drivers | Gathering as much information about what the stakeholders ,expect in the system. Include high-level functional requirements, business constraints, technical constraints, and quality attributes. |
| Document the Operation | Document and uses templates designed to capture information about the system architectural drivers include high-level functional requirements, business constraints, technical constraints and quality attributes. |

Table 2: Stage description

**Input:** N/A

**Output:** Operation document

### Stage 2

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
| Planning |  | Planning the activities of the stage and updating the master design plan to reflect the time that the architecture design team estimates they will take in stage 2. |
| Analyze Raw Architecture Drivers | analyze the consolidated raw architecture drivers information gathered in stage 1 to clarify and refine the architectural drivers |
| Review | After the architecture drivers specification is complete must review and formally accepted by the stakeholders. |
| Establish the scope of the system/product | Establish the scope, context, and size of the development effort. |

Table 3: Stage 2 description

**Input:** Operation document

**Output:** Architecture driver specification

### Stage 3

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
| Planning |  | Planning meeting for activity in this phase and update master plan about estimation time that completed design architecture phase |
| Design Architecture | The first time, design team will design architecture base on architecture driver specification from stage 2 |
| Refining Architecture | Design team will refine architecture design base on result evaluation from stage 4 |
| Update the Master Plan | When architecture design phase is finished, update master plan about actual time that completed design architecture phase |

Table 4: Stage 3 description

**Input:** Architecture driver specification

**Output:** Architecture design

### Stage 4

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
| Updating the master design plan |  | Updating the master design plan should occur after the stage is planned, to record the estimated time and resources required in stage 4. |
| Evaluation preparation | These are the activities associated with preparing for the architecture design evaluation workshop. |
| Evaluation workshop | This is the amount of time spent in the actual design evaluation. Typically ACDM evaluation lasts a day or less; however, in industry trials a few evaluations span two days for large systems with large external stakeholder groups |
| Post-evaluation activities | After the evaluation, the issues uncovered during the evaluation must be recorded in the issues action document, and the resolution action determined by the chief architect |

Table 5: Stage 4 description

**Input:** Architecture driver specification

**Output:** List issue recorded

### Stage 5

|  |  |  |
| --- | --- | --- |
| **Steps** | **Process** | **Description** |
| 1. planning |  | Managing engineer estimating the duration and resources required for the issue analysis meetings. |
| 1. Issue analysis meetings | Evaluate the list of issues uncovered in architecture evaluation (stage 4) and determine how each issue will be addressed.  Make a go/no-go decision. A go decision means the architecture is fit and ready for production; a no-go decision means that the architecture needs further refinement. |
| 1. Update the master design plan | At the conclusion of the evaluation, the master design plan is updated with the actual time and resources expended during stage 5. |

Table 6: Stage 5 description

**Input:** List issue recorded

**Output:** decision Go or No-Go

### Stage 6

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
| Experimentation planning |  | Responsible engineers creating experimentation plans to address each issue deposition established in stage 5. The experimentation plans are short  descriptions of how the issues will be resolved. |
| Experimentation | The responsible engineers will conduct the experiments according to the experimentation plans. The responsible engineers will also update the experimentation plans with actual performance data and experimentation results as the information is available. |
| Experimentation review meetings | This meeting is conducted by the architecture design team to share and review the results of the experiments and provide an opportunity to allow team members to provide comment on the various experiments |
| Update the master design plan | At the conclusion of stage 6, the master design plan is updated with the actual time and resources expended on experimentation. |

Table 7: Stage 6 description

**Input:** decision No-Go

**Output:** results of the experiments

### Stage 7

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
| Planning |  | Stage 7 planning involves determining the amount of time that the architecture design team anticipate they will spend developing the production schedule and reviewing the architecture design with the production engineers |
| Architecture Familiarization Workshop | The downstream detailed designers and implementers will understand the architecture design at varying levels of detail, depending upon their relationship with the architecture design team. |
| The Production Schedule | ACDM prescribes estimating the size, effort, and resources associated with producing each element of the architecture and then rolling up the element estimates into an overall system production estimate |
| Wideband Delphi | This is estimation methods that are used to estimate project costs and duration |
| Test Planning | During production planning, the requirements engineer must create plans for testing the system or product. Integrated system or product test should be planned by the quality process engineer, chief scientist, and requirements engineer. |
| Updating the Master Plan | At the conclusion of production planning, the managing engineer should update the estimated time spent in the architecture design familiarization meeting, and estimation, scheduling, and planning activities with actual performance. |

Table 8: Stage 7 description

**Input:** decision Go

**Output:** production schedule

### Stage 8

|  |  |  |
| --- | --- | --- |
| **Step** | **Process** | **Description** |
| re-gathering requirement |  |  |
| design architect ,structure in low level |  |
| Coding | implement coding follow detail design |
| Testing | test implemented |

Table 9: Stage 8 description

**Input:** production schedule

**Output:** product

# **Architecture Schedule**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PHASE | TASK NAME | START | FINISH | RESOURCES NAME |
| Architect & Design | create architecture plan | 18/11/2013 | 27/11/2013 | Ta Ngoc Thien Phu |
| system context | 31/12/2013 | 31/12/2013 | Deadline team |
| Develop physical view for admission system (high level) | 31/12/2013 | 4/1/2014 |  |
| Develop dynamic view for admission system (high level) | 31/12/2013 | 4/1/2014 |  |
| Develop static view for admission system (high level) | 31/12/2013 | 4/1/2014 |  |
| mapping physical with dynamic | 5/1/2014 | 6/1/2014 |  |
| mapping static with dynamic | 5/1/2014 | 6/1/2014 |  |
| Evaluate architect and design for admission system | 7/1/2014 | 9/1/2014 | Deadline team |
| review architect and design with Mr.Quang | 10/1/2014 | 17/1/2014 | Deadline team |
| update architecture design | 18/1/2014 | 23/1/2014 | Deadline team |
| Create sprint backlog | 24/1/2014 | 25/1/2014 | Deadline team |

# **Role and Responsibilities**

## Responsibility

### Managing Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Create Master Plan  - Support RE to planning about collect architecture drivers  - Tracking efforts base on  - Update and replan master design plan that base on actual data |
| 2 | - Update and replan master design plan that base on actual data |
| 3 | - Update and replan master design plan that base on actual data  - Unified plan with Chief Architect of the design stage |
| 4 | - Update and replan master design plan that base on actual data  - Unified and resolved issue about design |
| 5 | - Update and replan master design plan that base on actual data  - Celebrate meeting to decide go/ no go |
| 6 | - Update and replan master design plan that base on actual data  - participate same experiment |
| 7 | - Update and replan master design plan that base on actual data  - Ensure task progress and relation document |
| 8 | - Update and replan master design plan that base on actual data |

Table 10: Managing engineer responsibility

### Chief Architect

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Coordinate with RE to find and define requirement from stakeholder  - Elicit architecture drivers for RE  - Support RE write raw architecture driver document |
| 2 | - Lead analyze architecture drivers |
| 3 | - Lead all activities about architecture design  - Create architectural desgin document  - Support QPE about evaluation  - Coodunate with ME to planning in phase 3 |
| 4 | '- Review architecture design document and answer architecture question in phase evaluation |
| 5 | - Propose solutions to solve the problems encountered in meeting |
| 6 | - Working with responsible engineer for the issue to resolve the problem from the technical perspective  - Participate to experimentation if necessary |
| 7 | - Presents architectural design to detail design team  - Support the managing engineers to implement wideband delphi  - Based on estimated results for define development schedule |
| 8 | - Support for the designer detail  - Helps to production engineers understand the architectural design  - Ensure production on architecture design |

Table 11: Chief Architect responsibility

### Requirement Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Planning for this stage  - Coordinate and easily facilitate to get architecture drivers  - Establish meetings  - Write architecture drivers document |
| 2 | - Suppor analyze to architectural drivers  - Focus on technical issues  - Identify technical risks related to architectural drivers |
| 3 | - Manage requirements changes in the design  - Maintain communication with the stakeholders  - Support for CA in design, writing / updating the architectural design document  - Assistance QPE to evaluate |
| 4 | - Participate evaluate as questioner |
| 5 | - Participate in meetings to analyze problems  - Track issues that were given  - Mapping between requirement and issues  - Resolve problems |
| 6 | - Monitoring the change with stakeholders and the development has been break down in architectural drivers    - Participate to experimentation if necessary and resolve their effects |
| 7 | - Support ME to estimation method based on wideband delphi and develop schedule  - Responsible planning integration, testing, system / product |
| 8 | - Responsible for implementation / support integrate system and test system / product |

Table 12: Requirement Engineer responsibility

### Chief Scientist

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | ' – Working with RE to gather requirements    - Support the technical requirements    - Recognite raw Architectural drivers |
| 2 | - Suppor analyze to architectural drivers  - Focus on technical issues  - Identify technical risks related to architectural drivers |
| 3 | - Support CA to architectural design  - Concerned to technologies issues that affect architecture  - Assistance QPE to evaluate  - Support CA to create and update architectural design document |
| 4 | '- Support CA to research and answer the questions  - Participate in the evaluation as questioner |
| 5 | - Working with CA in meeting to analyse problem  - Propose ways to resolve the problem |
| 6 | - Work with responsible engineer for the issue to resolve the problem from the technical perspective  - Participate in testing if necessary |
| 7 | Present architecture driver for detail design team  - Support ME to estimation method based on wideband delphi and develop schedule  - Based on estimated results for define development schedule |
| 8 | - Support detail design team and develop team about technical |

Table 13: Chief Scientist responsibility

### Quality Process Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Ensure implement ACDM is correct  - Support RE to architectural drivers |
| 2 | - Ensure implement ACDM is correct  - Support RE to architectural drivers |
| 3 | - Đảm bảo ACDM thực hiện đúng  - Support to review architecture design document  - Support CA to completed architecture design document |
| 4 | - Ensure implement ACDM is correct  - Participate in the evaluation as questioner  - Review architecture design evaluation |
| 5 | - Participate issue analysis meeting  -Save evaluation document |
| 6 | - Ensure resolve all issue |
| 7 | - estimate wideband Delphi and develop implementation schedule  - Responsible planning integration, testing, system / product |
| 8 | - Monitoring Integrate system / product  - Ensure defect must be recognized |

Table 14: Quality Process Engineer responsibility

### Support Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Work with the requirements engineer to elicit the requirements from the stakeholders.  - Install, configure, and maintain the tools necessary to support stage 1 activities and any tools that can be established now to support the remainder of the project. |
| 2 | -Support to analyse and sum raw architectural drivers and write architectural drivers specification |
| 3 | -Support CS to design and write / update the architectural design document.  Process engineer to support quality assessment |
| 4 | - Participate in the evaluation as questioner |
| 5 | -Participate meetings to analyze issue |
| 6 | -Support Engineer is responsible for their experiments.  -Join the experiment as a responsible engineer if necessary |
| 7 | -Supports CA to present architectural design for detail design team and develop team.  Supports ME to estimate Wideband Delphi and base on it to develop of schedule |
| 8 | - Support production engineers and detail design team with any necessary tools for detailed design, implementation, or testing. |

Table 15: Support engineer responsibility

### Production Engineer

|  |  |
| --- | --- |
| **Stage** | **Description** |
| 1 | - Orientation hardware and software, architectural drivers document |
| 2 | - Analyze archtectural drivers |
| 3 | -Support the CS for the design and write / update the architectural design document.  Support QPE in evaluation |
| 4 | - Participate in the evaluation as questioner |
| 5 | -Participate assessed |
| 6 | - Participate in the experiment |
| 7 | - Participate in architectural presentation    - Ensure clear design |
| 8 | - Participate to support design |

Table 16: Product Engineer responsibility

## Role

|  |  |  |
| --- | --- | --- |
| **No** | **Roles** | **Members applied** |
| 1 | Managing engineer: | Chau Le |
| 2 | Support engineer | Huy Ngo |
| 3 | Chief architect | Phu Ta |
| 4 | Requirements engineer | Khang Huynh |
| 5 | Chief scientist | Dao Khau |
| 6 | Quality process engineer | Huy Nguyen |
| 7 | Production engineers | All team |

Table 17: Role